

VadaTech UTC007/UTC008

# User's Manual

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## Revision History

Doc Rev	Description of Change	Revision Date
1.0.0	Document Created	9/30/2010

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# 1 Overview

This document describes the VadaTech UTC007/UTC008 products and their use as a JSM switch for the VT86X VadaTech Chassis. These products feature the Maxim 16 port DS26900 JSM switch.

The UTC007 and UTC008 feature one 10 pin .1 header.

## 1.1 Applicable Products

- VadaTech UTC007
- VadaTech UTC008

## 1.2 Document References

- N/A

## 1.3 Acronyms Used in this Document

Acronym	Description
JSM	JTAG Switch Manager
ATCA	Advanced Telephony Computing Architecture
DIP	Dual In-line Package
GND	Ground
LED	Light Emitting Diode
μTCA	Micro Telephony Computing Architecture
JTAG	Joint Test Access Group

Table 1: Acronyms



## 2 Hardware

### 2.1 Hardware Common to Each Board

LEDs behave as follows:

LED	OFF	ON
ACT	JSM is OFF	JSM is active
Slave Select 1,2,4,8,16	Not Selected	The combination of LEDs ON will tell you which port is selected as the slave for JTAG use.
MGNT 0, 1, 2	Not Selected	The LED that is ON is the management port.
MC	No conflict	Master Conflict has occurred
DPDV	Bit not set	Bit for Deselect Port Data Value in DCR is Set

Table 2: UTC007/UTC008 LED Behavior

**NOTE:** The card is not hot swappable and should only be removed when the carrier is powered off.

To insert the card, pull out the handle until it stops. Locate the JSM slot in the chassis. Insert the card into the carrier's JSM slot guide rails and push on the front panel firmly until it is fully seated into the connector. If the card does not go fully in, do not force it and instead remove it and check for proper orientation or obstructions. Once fully inserted the Active LED should go to solid red.

To remove the card when the chassis is powered off, pull out the handle until it stops to unlatch the card from the carrier. Then continue pull the handle straight out firmly to remove the card from the carrier.

SWITCHES	Meaning
CFG	Configuration: Turn ON to put the JSM in configuration mode
FTM REQ	Test Master Request: Turn ON to activate Master Request

SW3 position 1	Meaning
OFF	Front panel JTAG port selected
ON	Backplane JTAG port selected

Table 3: SW3 Master JTAG port selection

SW3 Position #	Definition	Meaning	
2	Front JTAG Port Pin 4	OFF	No connect
		ON	+3.3V
3	Front JTAG Port Pin 6	OFF	No connect
		ON	+3.3V
4	Front JTAG Port Pin 7	OFF	No connect
		ON	+3.3V

Table 4: SW3 Front panel pin assignment

## 2.2 UTC007/UTC008 Hardware

The UTC007 and UTC008 board layout and front panel are shown below for reference:

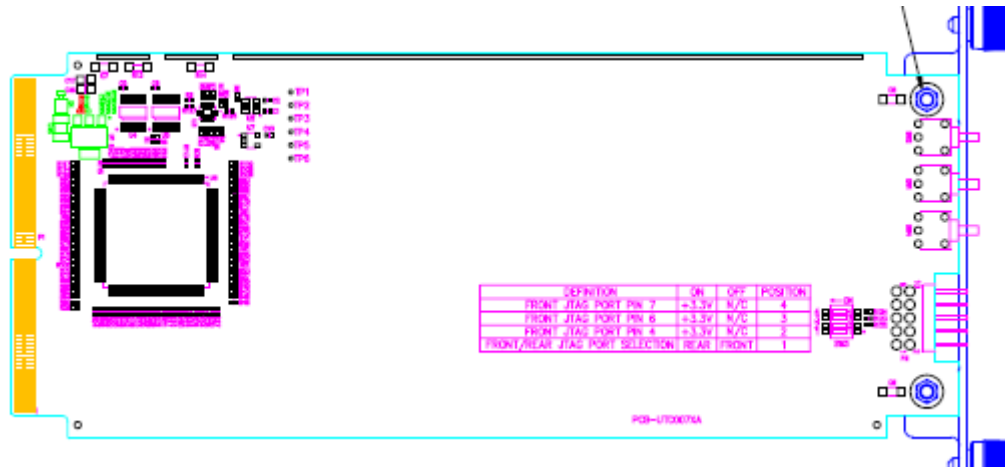


Figure 1: UTC007 board layout

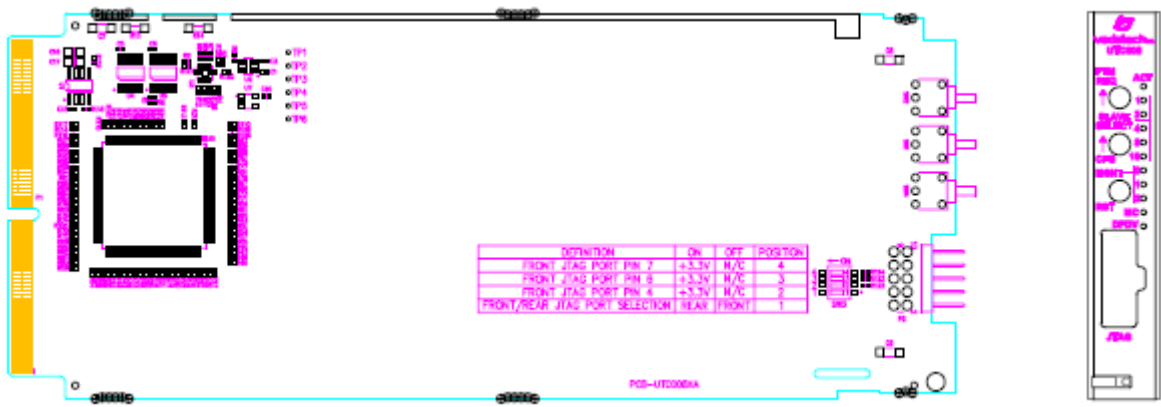


Figure 2: UTC008 board layout



Figure 3: UTC00X front panel

The UTC00X has a 10 pin header so that a custom cable can be created to match your JTAG probe pins. This 10 pin header is pinned out as:

Pin Number	Description
1	TCK
2	GND
3	TDO
4	Selectable by SW3 to +3.3V
5	TMS
6	Selectable by SW3 to +3.3V
7	Selectable by SW3 to +3.3V
8	TRST
9	TDI
10	GND

Table 5: 10 Pin Header Pin Out

## 3 Configuration Files for DS26900

### 3.1 Product Summary

The UTC007 and UTC008 boards are used for JTAG across the uTCA backplane.

### 3.2 Using XILINX Interface for Configuration

Use this BSD file for initializing the JSM device in the Xilinx Impact tool:

```
entity generated_ds26900cfg is

generic (PHYSICAL_PIN_MAP : string := "X_PACKAGE");

port (TCK: in bit; TDI: in bit; TDO: out bit; TMS: in bit);

use STD_1149_1_2001.all;
attribute Component_Conformance of ds26900cfg : entity is "STD_1149_1_2001";

attribute PIN_MAP of ds26900cfg : entity is PHYSICAL_PIN_MAP;

constant X_PACKAGE:PIN_MAP_STRING := "TCK : 1," & "TDI : 2," & "TDO : 3," &
"TMS : 4";
attribute Tap_Scan_In of TDI: signal is true;
attribute Tap_Scan_Mode of TMS: signal is true;
attribute Tap_Scan_Out of TDO: signal is true;
attribute Tap_Scan_Clock of TCK: signal is (1.0e06, BOTH);

attribute Instruction_Length of ds26900cfg: entity is 5;
attribute Instruction_Opcode of ds26900cfg: entity is "BYPASS (11111)";
attribute Instruction_Capture of ds26900cfg: entity is "XXX01";
attribute Boundary_Length of ds26900cfg: entity is 1;
attribute Boundary_Register of ds26900cfg: entity is "0 (BC_1, *, control,
0)";

end ds26900cfg;
```

Use this SVF file to configure the JSM to target a specific slot of the chassis for JTAG:

```

TRST OFF;
ENDIR IDLE;
ENDDDR IDLE;
STATE RESET;
STATE IDLE;
FREQUENCY 1E6 HZ;

// read idcode register
SIR 5 TDI (00) SMASK (1f) ;
SDR 8 TDI (00) SMASK (ff) TDO (c0) MASK (ff) ;

// write to GPIOCR register
//   GPIO0 = out 0
//   GPIO1 = out 1
//   GPIO2 = out 0
//   GPIO3 = out 1
SIR 5 TDI (03) SMASK (1f) ;
SDR 8 TDI (99) SMASK (ff) TDO (00) MASK (00) ;

// write to SPSR register to select secondary port
// Changing the value of TDI will select which port on the chassis is
// connected
// to the JSM switch
SIR 5 TDI (01) SMASK (1f) ;

//   TDI = 0x01 = select secondary port 1
//   TDI = 0x02 = select secondary port 2
//   etc.
//   TDI = 0x0C = select secondary port 12

SDR 5 TDI (01) SMASK (1f) TDO (00) MASK (00) ;

```

This example above configures to port 1. To configure to port 2, use the highlighted changes:

```

SIR 5 TDI (02) SMASK (1f) ;
//   TDI = 0x01 = select secondary port 1
//   TDI = 0x02 = select secondary port 2
//   etc.
SDR 5 TDI (02) SMASK (1f) TDO (00) MASK (00) ;

```

For selecting port 12, use the highlighted values:

```

SIR 5 TDI (0C) SMASK (1f) ;
SDR 5 TDI (0C) SMASK (1f) TDO (00) MASK (00) ;

```

This is a sequence of pictures that step through using the VadaTech JSM with the Xilinx impact tool to communicate with the MAXIM DS26900 and then configure it for JTAG operation.

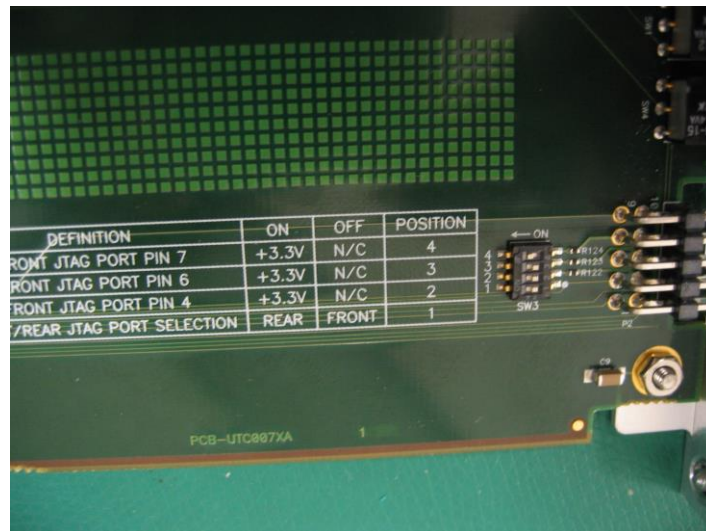


Figure 4: Switch settings for selecting Port Routing

The FTM REQ and CFG switches must be turned ON to do these configuration steps. When finished turn the CFG switch OFF to be able to do normal JTAG transactions.

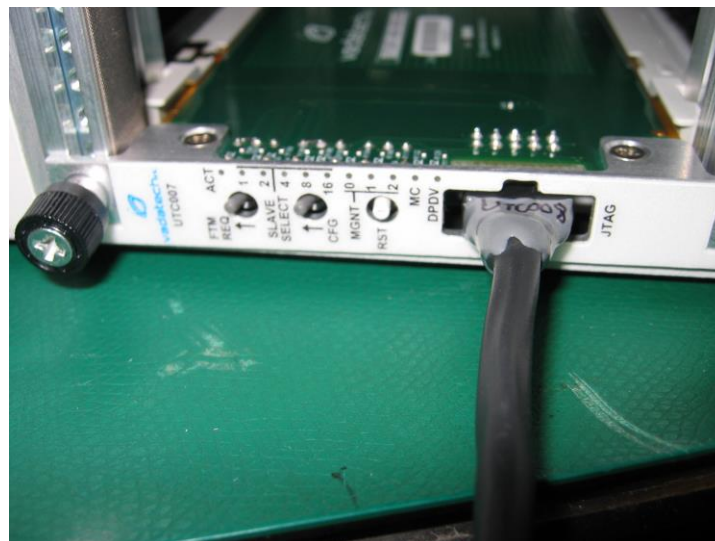


Figure 5: Front Panel Settings

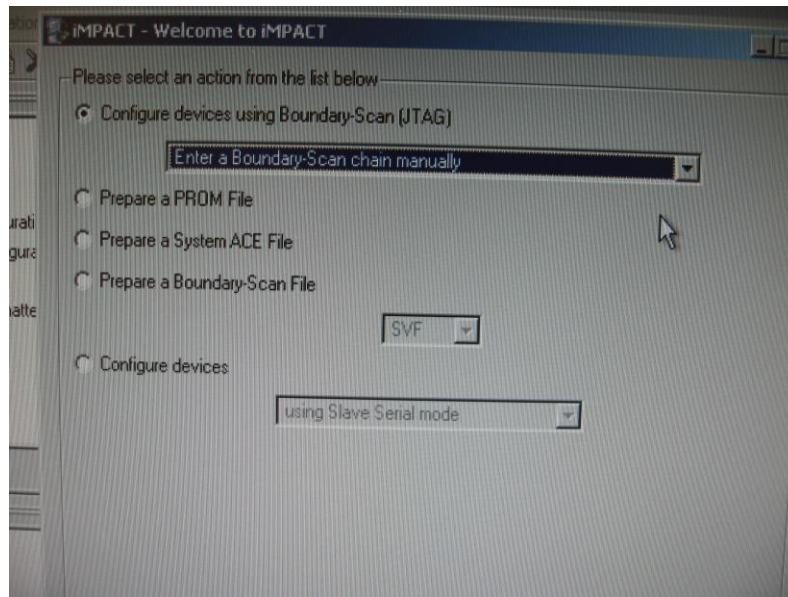


Figure 6: Selecting Device with Xilinx Impact

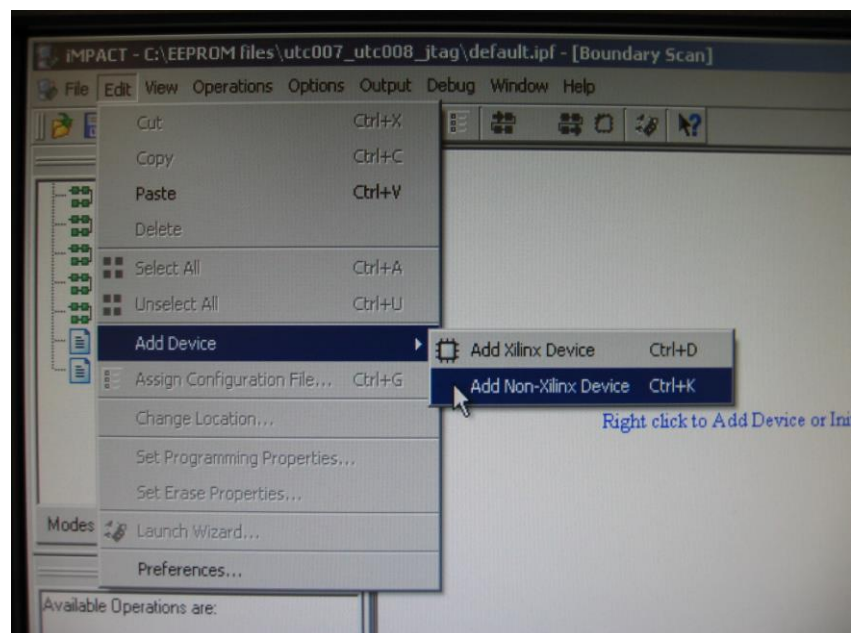


Figure 7: Add Non-Xilinx Device with Xilinx Impact



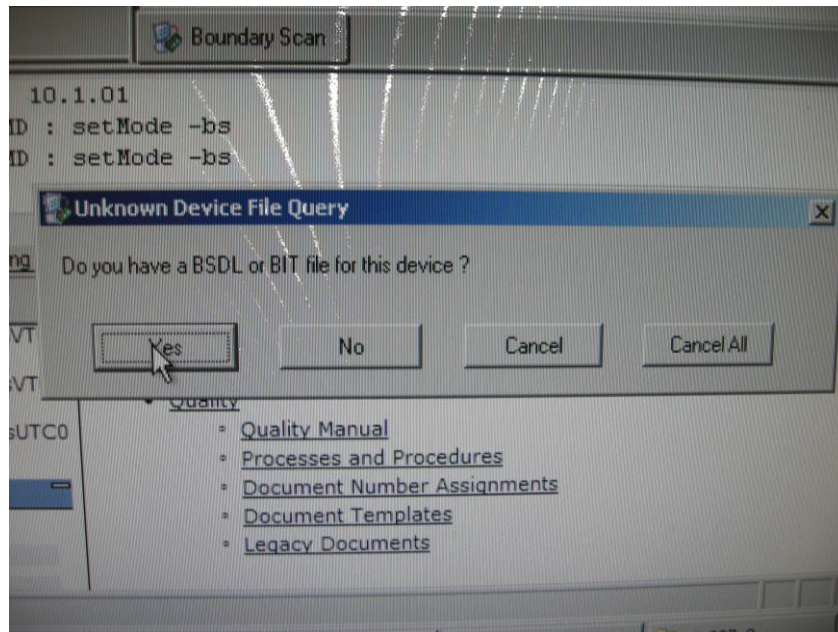


Figure 8: Add BSD with Xilinx Impact

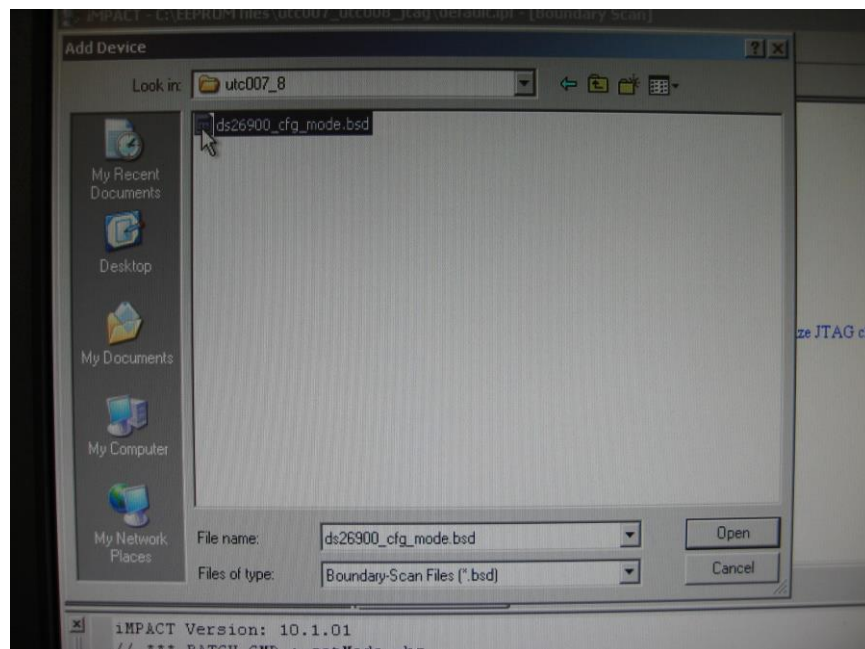


Figure 9: Using ds26900\_cfg\_mode.bsd with Xilinx Impact

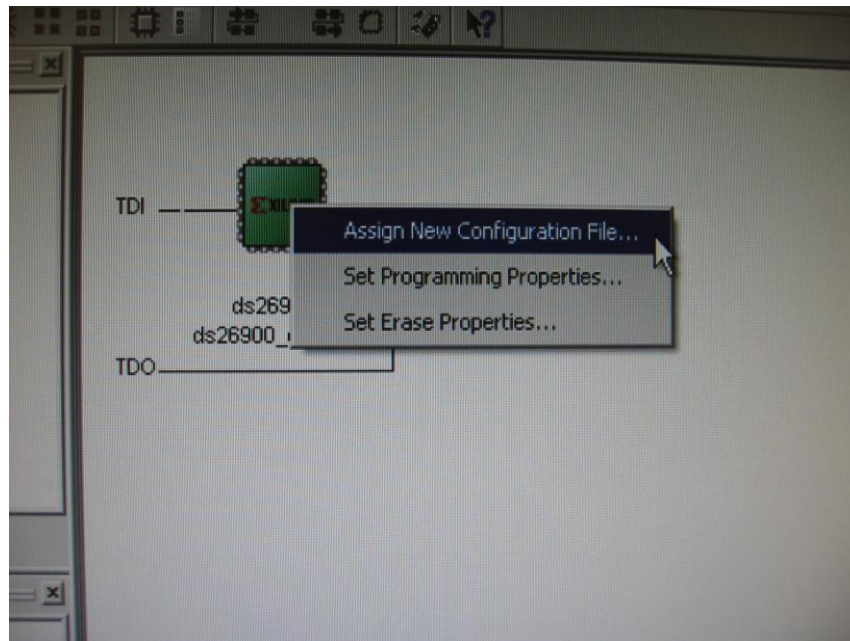


Figure 10: Loading a vector file with Xilinx Impact

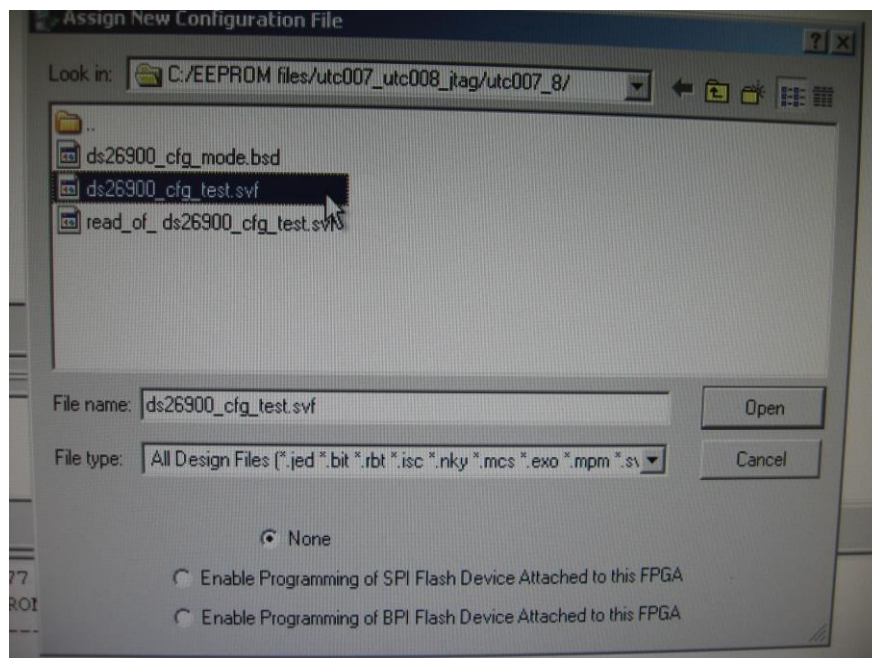


Figure 11: Select correct vector file with Xilinx Impact

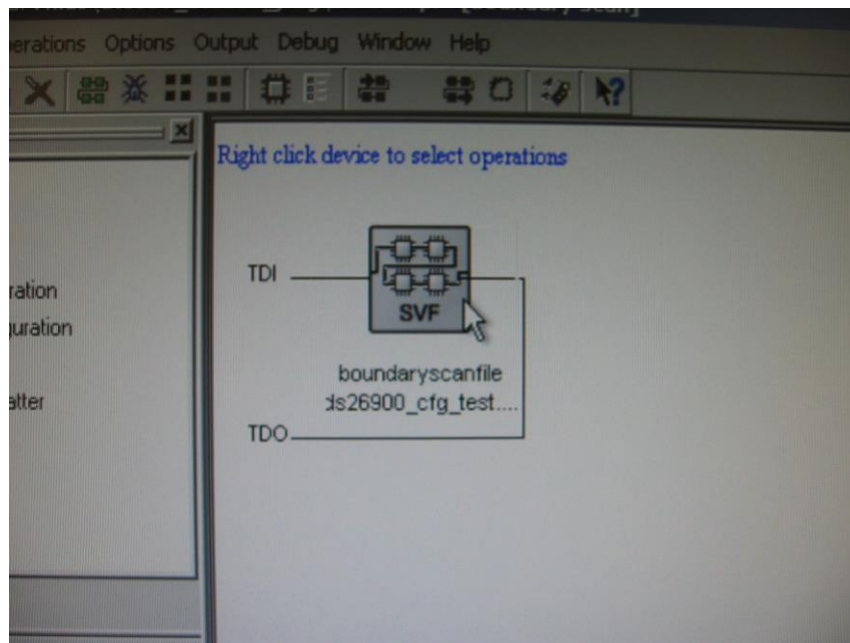


Figure 12: Execute the vector file with Xilinx Impact

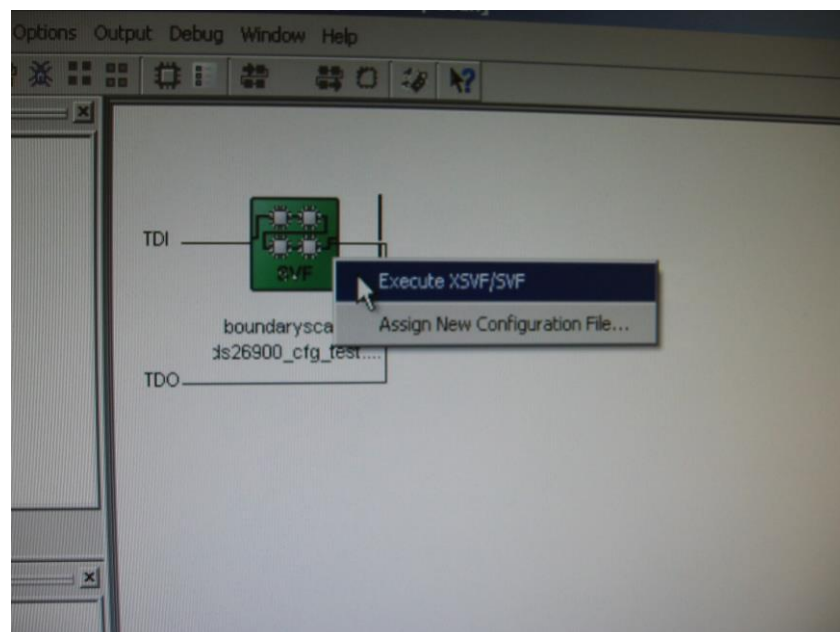


Figure 13: Start vector file with Xilinx Impact

If it is successful a play succeeded will be displayed. You turn OFF the CFG switch to start making JTAG transactions.